CLAIMS

What is claimed is:

1. (Currently Amended) A unified tag subsystem for a multilevel cache memory system having an upper level and a lower level of cache data memory, the tag subsystem having at least a processor port for receiving a cache line address comprising a tag index portion, and a high order part, the unified tag subsystem comprising:

a unified tag memory coupled to be addressed by the tag index portion of the cache line address, the tag memory comprising at least one way-specific address tag, at least one upper level valid flag, and at least one way-specific lower level flag;

at least one first comparator coupled to compare the high order part with the at least one way-specific address tag and detect a match;

a lower level hit logic coupled to determine a lower level cache hit when the at least one first comparator detects a match, and the lower level flag of the tag memory indicates a valid entry in the lower cache; and

an upper level hit logic coupled to determine a higher level cache hit when the at least one first comparator detects a match, and a high level valid flag of the tag memory is in a valid state.

2. (Original) The unified cache tag subsystem of Claim 1, wherein there are at least two way-specific address tags, and at least two first comparators.

3. (Original) The unified cache tag subsystem of Claim 2 wherein the unified cache tag subsystem further comprises cache coherency maintenance logic coupled to the tag memory subsystem.

4. (Original) The unified cache tag subsystem of Claim 3, wherein the coherency maintenance logic is cache snoop logic.

5. (Original) The unified cache tag subsystem of Claim 1 wherein the at least one way-specific lower level flag comprises information indicating a way of storage in lower level data memory at which cache data may be located.

6. (Original) The unified cache tag subsystem of Claim 5, wherein there are a plurality of first comparators for multiple ways of associativity.

7. (Original) A multilevel cache memory system having at least a processor port for receiving a cache line address comprising a tag index portion, and a high order part; the multilevel cache memory system comprising:

a lower level cache data memory coupled to provide data to the processor port on a lower level cache hit;

an upper level cache data memory coupled to provide data to the processor port on an upper level cache hit;

a unified tag subsystem further comprising:

a tag memory coupled to be addressed by the tag index portion of the cache line address, the tag memory comprising at least one way-specific address tag field, at least one way-specific lower level flag field, and at least one way-specific upper level valid flag;

at least one comparator coupled to compare the high order part with the at least one way-specific address tag and detect a match;

a lower level hit logic coupled to determine a lower level cache hit when the at least one first comparator detects a match and the lower level flag indicates valid cache data in the lower level cache data memory; and

an upper level hit logic coupled to determine a higher level cache hit when the at least one first comparator detects a match, and the a higher level valid flag field indicates valid cache data in a upper level cache data memory.

8. (Original) The cache system of Claim 7, wherein the higher level valid flag field comprises a plurality of higher level valid flags, and wherein each higher level valid flag indicates validity of data in a line of a superline in upper level cache data memory.

9. (Original) The multilevel cache memory system of Claim 7 wherein a cache line of the lower level cache data memory is smaller than a cache line of the upper level cache data memory, wherein lower level cache data memory has

fewer ways of storage than the upper level cache data memory, wherein the lower level flag field of the unified cache tag subsystem further comprises a plurality of lower level flags, wherein the lower level flags indicate ways of storage in lower level cache data memory where corresponding data is located in lower level cache data memory.

10. (Original) The multilevel cache memory system of Claim 7, wherein the multilevel cache memory system further comprises cache coherency maintenance logic.

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11. (Original) The multilevel cache memory system of Claim 7, wherein the upper level valid flags of the cache tag memory subsystem further comprise a plurality of way-specific superline segment valid flags, and wherein each superline segment valid flag contains validity information for an upper level cache line of an upper level cache superline, and wherein the upper level cache data memory is capable of storing a plurality of superlines.

12. (Original) The multilevel cache memory system of Claim 7, wherein the unified tag subsystem further comprises way limit apparatus whereby specific ways of storage may be disabled.

13. (New) A multilevel cache memory system having at least a processor port for receiving a cache line address comprising a tag index portion, and a high order part; the multilevel cache memory system comprising:

a lower level cache data memory coupled to provide data to the processor port on a lower level cache hit;

an upper level cache data memory coupled to provide data to the processor port on an upper level cache hit;

a unified tag subsystem further comprising:

a tag memory coupled to be addressed by the tag index portion of the cache line address, the tag memory comprising at least one way-specific address tag field, at least one way-specific lower level flag field, and at least one way-specific upper level valid flag;

at least one comparator coupled to compare the high order part with the at least ne way-specific address tag and detect a match;

a lower level hit logic coupled to determine a lower level cache hit when the at least one first comparator detects a match and the lower level flag indicates valid cache data in the lower level cache data memory;

an upper level hit logic coupled to determine a higher level cache hit when the at least one first comparator detects a match, and the a higher level valid flag field indicates valid cache data in a upper level cache data memory; and

wherein the upper level data cache is larger and slower than the lower level data cache.